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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,785	04/13/2004	Ramin Ghodsi	M4065.0900/P900	3196

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EXAMINER	
WENDLER, ERIC J	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/822,785	GHODSI, RAMIN	
	Examiner	Art Unit	
	Eric Wendler	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search History*.

DETAILED ACTION

1. This action is responsive to the following communications: the Application filed on April 13, 2004.

2. Claims 1-22 are pending in the case. Claim 1, 4, 10, 14, 17, 18, 19, 21, and 22 are independent claims.

Information Disclosure Statement

3. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609.04(a) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Drawings

4. **Figure 2** should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 10-11, 13 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by the US Patent to Nejad et al (6,940,748).

6. **Regarding claims 10-11, and 13,** Nejad teaches, in Figs. 1-2, a two-dimensional array of resistive memory elements that are MRAM elements (**38**) disposed in a parallel spaced relation between a second two-dimensional array of resistive memory elements and a two-dimensional array of isolation devices (**12**), each isolation device being coupled to at least one resistive memory element in each of the two two-dimensional arrays of resistive memory elements. Nejad also teaches a plurality of read/write conductors (**44**) having respective longitudinal axes oriented in a first direction and coupled to the first two-dimensional array of resistive memory elements; and a second plurality of read conductors (**33**) having respective longitudinal axes also oriented in the first direction and also coupled to the first two-dimensional array of resistive memory elements. While this specific teaching may not explicitly evident, upon further examination of the figures and the specification, it can be seen that a figure of the MRAM array shown as a two-dimensional drawing of the X and Y-axes would look like Figs. 4A-4B of the present application. Nejad further teaches a sensing

circuit (**50**) adapted to sense a state of the resistive memory elements during a time interval when a respective isolation device is activated.

7. **Regarding claim 17,** Nejad teaches, in Figs. 1-3, a semiconductor substrate (**10**) having an upper surface; a controlled transistor (**16**) having a drain region (**14**) disposed on said semiconductor substrate; magnetic random access memory storage elements disposed above the upper surface and above the drain region in spaced relation thereto and electrically coupled to the drain region through read conductors (**33**) having longitudinal axes; and read/write conductors (**44**) having longitudinal axes substantially parallel to those of the read conductors. While this specific teaching may not explicitly evident, upon further examination of the figures and the specification, it can be seen that a figure of the MRAM array shown as a two-dimensional drawing of the X and Y-axes would look like Figs. 4A-4B of the present application.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over the US Patent to Nejad et al (6,940,748) and the US Patent Application to Nahas (2005/0216244).

10. **Regarding claims 1, 2, and 4,** Nejad teaches, in Figs. 1-3, a magnetic random access memory cell (**38**) comprising a magnetic storage elements having a sense layer (**43**) and a pinned layer (**41**), the sense layer mutually electrically coupled to a read conductor (**33**) and the pinned layer coupled to a read/write conductor (**44**), with longitudinal axes parallel to each other. Nejad fails to explicitly teach that the memory cell includes exactly two resistive memory elements. However, Fig. 1 shows what would be an equivalent structure known in the art. Therefore, because these two are art-recognized equivalents at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute a memory cell with one resistive memory element for a memory cell with exactly two resistive memory elements. Nejad also teaches a switching device with a first controlled terminal coupled to the pinned layers through a read conductor and a control terminal adapted to receive a control signal. Nejad fails to explicitly teach the source of the switching device connected to a ground potential, but it would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the source of the switching device to a ground potential as it is well-known in the art to do this, as evidenced by the teaching of Nahas. Nahas teaches, in Fig. 1, a second controlled terminal (**124**) of a controlled transistor (**130**) coupled to a source of constant potential which is shown to be a ground potential (**115**).

11. **Regarding claim 3,** Nejad further teaches that the stacked magnetic storage elements are disposed above the switching device in a first direction, and

the switching device is disposed beside a further switching element of a further magnetic random access memory cell in a second direction.

12. **Regarding claims 5-6,** Nejad teaches all the claimed elements as discussed above, including the fact that the resistive memory elements include pinned layers and sense layers are electrically coupled through the controllable transistor. Nejad fails to explicitly teach the source of the switching device connected to a ground potential, but it is well known in the art to do this, as evidenced by the teaching of Nahas. Nahas teaches, in Fig. 1, a second controlled terminal of a controlled transistor coupled to a source of constant potential which is shown to be a ground potential.

13. Claims 7-9, 12, 16, and 18-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over the US Patent to Nejad et al (6,940,748) in view of the US Patent to Hush et al (6,791,859).

14. **Regarding claim 7,** Nejad teaches all the claimed elements as discussed above, but fails to teach that the controllable transistor comprises two transistors sharing a common drain connection and respective gate terminals mutually coupled to one another. Hush teaches, in Fig. 1, a controllable transistor that comprises two transistors sharing a common drain connection and respective gate terminals mutually coupled to one another. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to substitute the single transistor of Nejad with the dual transistor of Hush as this allows the array to be implemented in a smaller area.

15. **Regarding claim 8,** Nejad further teaches the resistive memory elements disposed in layered spaced relation to one another above the controllable transistor.

16. **Regarding claim 9,** Nejad teaches all the claimed elements as discussed above, but fails to explicitly teach a word line conductor electrically coupled to a gate of the controllable transistor, even though he does teach that the gate of the controllable transistor controls the reading of the memory cells. Hush teaches, in Fig. 2, a word line conductor electrically coupled to a gate of a controllable transistor. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to apply the teaching of Hush to the system of Nejad and connect a word line conductor to the gate of the controllable transistor, as this is a well-known way of controlling such a memory array.

17. **Regarding claims 12 and 18,** Nejad teaches all the claimed elements as discussed above but fails to teach that the resistive memory elements comprise PCRAM memory elements. Hush teaches an array of PCRAM devices as being resistive memory elements that can store binary data. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to substitute the MRAM structures of Nejad for the PCRAM structures of Hush as they are both types of resistive memory elements.

18. **Regarding claim 16,** Nejad teaches all the claimed elements as discussed above, but fails to explicitly teach an address decoder coupled to the dual transistor. Hush, in Fig. 2, further teaches an address decoder electrically coupled to the first and second gates of the dual transistor and adapted to

activate the dual transistor in response to an address signal received at an address input of the address decoder. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to use the address decoder of Hush with the elements taught by Nejad for the purpose of being able to control the addressing of the memory cells.

19. **Regarding claim 21,** Nejad teaches all the claimed elements as discussed above but fails to explicitly teach that the transistor is a wired-NOR FLASH memory style transistor. Hush teaches, in Fig. 1, the use of a dual transistor similar to those used in FLASH memories to couple the memory storage elements to a reference potential. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to substitute the single transistor of Nejad with the dual transistor of Hush as this allows the array to be implemented in a smaller area and at lower cost.

20. **Regarding claims 19-20, and 22,** they encompass the same scope of invention as that of claims 10 and 21 except they draft the invention in method format instead of apparatus format. Nejad and Hush teach all the necessary elements of the device formed by the process listed in claims 19-20 and 22. The aspects of the invention contained in claims 19-20 and 22 are therefore rejected in method format for the same reasons claims 10 and 21 were rejected in apparatus format, as set forth in the above paragraphs of the office action.

21. **Claims 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the US Patent to Nejad et al (6,940,748) in view of the US**

Patent to Hush et al (6,791,859) and the US Patent Application to Nahas (2005/0216244).

22. **Regarding claims 14-15,** Nejad teaches a plurality of memory cells with resistive memory storage elements electrically coupled to memory sensing circuits and mutually coupled to a reference potential through a transistor and disposed in spaced relation above the transistor. Nejad fails to explicitly teach the source of the switching device connected to a ground potential, but it is well known in the art to do this, as evidenced by the teaching of Nahas. Nahas teaches, in Fig. 1, a second controlled terminal of a controlled transistor coupled to a source of constant potential which is shown to be a ground potential. Nejad also fails to teach that the controllable transistor is a common dual transistor. Hush teaches, in Fig. 1, a controllable transistor that comprises two transistors sharing a common drain connection and respective gate terminals mutually coupled to one another. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to substitute the single transistor of Nejad with the dual transistor of Hush as this allows the array to be implemented in a smaller area.

Conclusion

23. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Sharma et al (6,850,433) teaches an MRAM memory element that is that same as the memory element claimed in the present application except the axes of the read and read/write conductors are not longitudinal in the same direction. Tuttle (6,903,396) teaches a system of

magnetic memory element arrayed in much the same way as the present application.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Wendler whose telephone number is (571) 272-5063. The examiner can normally be reached on Monday - Friday 8AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

1/9/06

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12/28/05